# OBC SIMULATORS
## Flight Computer Models

*An OBC Simulator is a simulation – or digital twin - of a real spacecraft flight computer. These are used in a variety of applications.*
*The most common are:*

- *Software Validation Facilities: For development and testing of flight software without the need of a real flight computer*

- *Operational Simulators: Used to simulate the spacecraft and other elements for the purpose of Mission Control Team Training, Flight Procedure Validation and Ground Segment Qualification*

In recent years, Terma have provided a number of models for Beyond Gravity flight computers

**beyond gravity**

https://products.beyondgravity.com/d/SVq1aavsDmtE/library?category07=Satellites&platform06=Electronics

**SUPPORTED COMPUTERS**

Currently three families of computer are supported:
- OBCs flown in missions such as MTG, SARah, Euclid
- New generation OBC used in PLATO – OBC-NG and CO2M
- Constellation Single Board Computer – cOBC

**THE SIMULATOR**

All redundancies, cross strappings and accurate timing are modelled.
SpaceWire, MIL-1553, CAN & OBDH Buses are modelled.
Simulation of two processors (A and B side), also running in dual boot, is supported.
The data storage part of the CREOLE ASIC can be selected to be modelled in RAM (4GB) or on files to disc (limited by hard disk size).
Modelling of external Solid-State Mass Memory is also supported if required
Failures are supported – for example model stops responding, power under/over voltage. More detailed modelling exists for the OBDH, 1553, SPW where more

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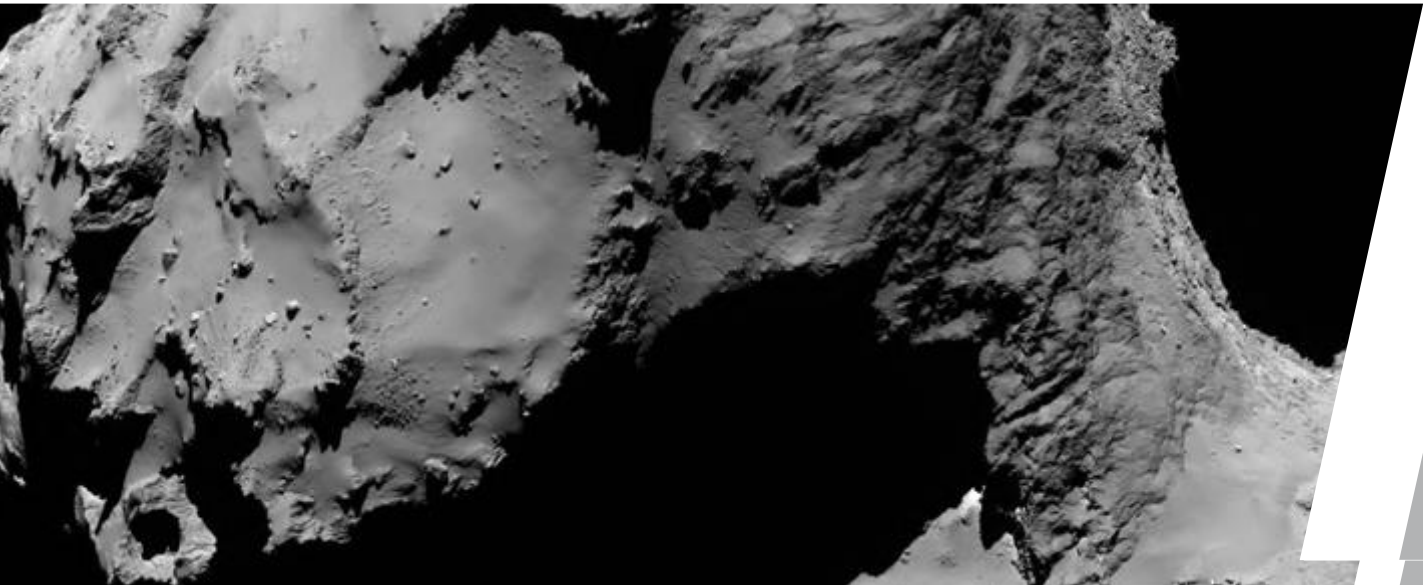
specific testing of the OBSW is required – e.g. - failing the 1553 Status response from a specific remote terminal

## ARCHITECTURE

The simulator is made up of a number of models. At the core is the processor emulator. This is surrounded by a variety of models simulating the ASICs (e.g. CREOLE, COLE, CROME2, HAMSTER, TTR, DS) and buses. Power and storage are also modelled. Optionally other items can also be provided as models, such as Remote Terminal Units (RTU), Solid State Mass Memory (SSMM), Authentication Unit (AU).

## TESTING

Testing of the model uses a two step process.
The models come with an SMP Simulation Testing Infrastructure used for automated unit, integration and system level testing.
For more hardware representative level testing, the same environment used to test the real hardware – the PyTE Test tool – is used to test the simulator. This includes the use of BeyondGravity Test Application Software (TASW).
The use of the PyTe tool covers a broad set of tests. The result is a very robust model that can then readily be integrated into a full simulator.

## PROCESSOR EMULATOR

The processor emulator at the core of the model is a Terma product - TEMU.

Continual investment is made to ensure it can support the latest processors used in the space domain.
The following processor models are included:

- SPARCv8 based ERC32, LEON2 (AT697), LEON3 (UT699, UT700 etc), LEON4 (GR740).
- ARMv7 support includes the TMS570
- PowerPC architecture is also supported (PPC750, P2020)

*Product Link:*
https://www.terma.com/space/space-segment/flight-processor-emulators/

## PERFORMANCE

The performance of the model is mainly driven by the performance of the emulator. For processors such as the ERC32, the emulator can achieve 50x real-time performance, for the LEON series performance over 10 times real-time have been observed on real flight-software.

## MODEL DEVELOPMENT

The environment in which the model is developed is Linux (various variants supported). The ESA/ESOC SIMULUS tools are used for the development, including the design. The models are developed to the SMP2/ECSS-SMP standard. This means they can be readily integrated into other simulators so users are not constrained to use the ESA tools – there are already several examples of this.
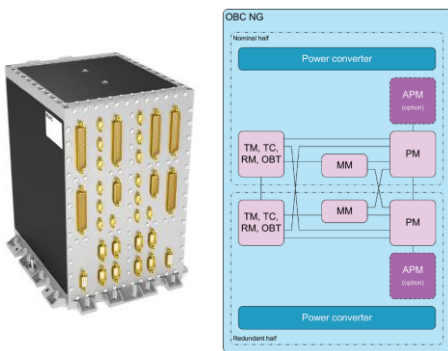


*The Computer*
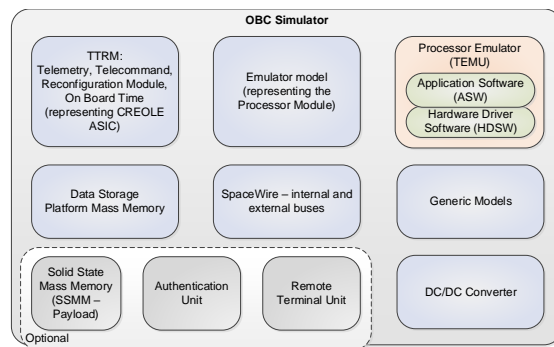


*Simulation Model*

**You are interested in a Spacecraft Simulator for your single Spacecraft or Constellation?**

Reach out to us for further information: terma.space@terma.com

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